FLASH MEMORY WITH DATA DECOMPRESSION

FIELD OF THE INVENTION

[0001] The present invention relates generally to data processing systems and in particular the present invention relates to initiation of data processing systems.

BACKGROUND OF THE INVENTION

[0002] Processing systems, or computers, typically include a processor and a memory device as internal storage areas for the computer. The term memory identifies data storage that comes in the form of integrated circuit chips. While there are several different types of memory, DRAM (dynamic random-access memory) is traditionally used as the main memory in a computer environment. With the development of different RAM's, a high-speed synchronous-type DRAM is often used with the processor. The dynamic memory, however, cannot retain data in the absence of power. As such, computer system contains some non-volatile storage device. For example, a magnetic storage device or non-volatile memory can be used to store data and software.

[0003] During operation, the processor copies data from the non-volatile storage to the dynamic memory. That is, the data from the non-volatile storage is routed via the processor to the dynamic memory. This process consumes power, is time consuming, and consumes processor bandwidth. In addition, the storage capacity of the non-volatile memory can limit the data available for transfer.

[0004] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a system and method which improves data transfer from a non-volatile storage device to a volatile storage device.

SUMMARY OF THE INVENTION

[0005] The above-mentioned problems with processing systems and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0006] In one embodiment, a processing system comprises a processor, a volatile storage device coupled to communicate with the processor, and a non-volatile memory device coupled to communicate with the processor and the volatile storage device. The non-volatile memory device transfers data to the volatile storage device and includes a decompression circuit to decompress the data while transferring to the volatile storage device.

[0007] In another embodiment, a processing system comprises a processor, a synchronous memory device coupled to communicate with the processor via a synchronous bus, and a flash memory device coupled to communicate with the processor via a serial bus and communicate with the synchronous memory device via a direct bus. The flash memory device transfers data to the synchronous memory device, and includes a decompression circuit to decompress the data while transferring to the synchronous memory device.

[0008] A processor system power-up method comprises detecting a power-up condition and providing a reset signal to a volatile memory, initiating a direct data transfer from a non-volatile memory to the volatile memory in response to the reset signal, decompressing data stored in the non-volatile memory while transferring the data to the synchronous memory, and providing a system reset signal from the volatile memory to a processor.

[0009] Another processor system power-up method comprises detecting a power-up condition with a reset controller and providing a reset signal to a synchronous memory, using the synchronous memory, initiating a direct data transfer from a flash memory to the synchronous memory in response to the reset signal, decompressing data stored in

the non-volatile memory while transferring the data to the synchronous memory, and providing a system reset signal from the synchronous memory to a processor after the data has been transferred.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 illustrates a block diagram of a flash memory device of an embodiment of the present invention; and

[0011] Figure 2 is a block diagram of a system of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0012] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

[0013] Figure 1 illustrates a block diagram of a flash memory device of an embodiment of the present invention. The memory device 100 includes an array of non-volatile flash memory cells 102. The array is arranged in a plurality of addressable banks. In one embodiment, the memory contains four memory banks 104, 106, 108 and 110. Each memory bank contains addressable sectors of memory cells. The data stored in the memory can be accessed using externally provided addresses received by address register 112. The addresses are decoded using row address decoder circuitry 114. To access an appropriate column of the memory, the received addresses are coupled to

column decode circuitry 122. Data is input and output I/O buffer 128. Command execution logic 130 is provided to control the basic operations of the memory device. A state machine 132 is also provided to control specific operations performed on the memory arrays and cells. A decompression engine 140 is provided in the memory, as explained below. A serial port 142 can be provided to communicate with an external storage device, as explained below.

[0014] Referring to Figure 2, an embodiment of a processing system of the present invention is described. The system includes a central processing unit (CPU) 200, or processor, that is coupled to a synchronous memory bus 202 and corresponding synchronous DRAM memory(ies) 204. The processor is also coupled to a synchronous flash memory 206. The synchronous DRAM (SDRAM) is coupled to the flash memory for copying data from the flash to the SDRAM during a power-up operation, as explained below. The synchronous memory, in another embodiment, is a Rambus® DRAM (RDRAM). The present invention is not limited to a DRAM based volatile memory. That is, the present invention can be implemented to transfer data from a non-volatile device, such as but not limited to a flash memory, EEPROM, or magnetic storage device, to any type of volatile storage device.

[0015] As further illustrated in Figure 2, the present invention includes a decompression engine 220. The decompression engine allows data transferred from the flash memory to the synchronous memory to be decompressed. The decompression hardware, in one embodiment, can decompress data having a compression ratio of 2:1. It will be appreciated by those skilled in the art with the benefit of the present description that additional compression ratios can be implemented. The data stored in the memory is compressed prior to writing the memory. That is, the memory contains decompression but not compression circuitry. The decompression circuitry can incorporate any type of decompression algorithm, including but not limited to a Lempel-Ziv compression algorithm, see for example United States Patent No. 4,558,302.

[0016] The present invention allows the non-volatile memory contents to be decompressed and loaded into the SDRAM. The processor can be used to load and update the data in the flash memory. The flash memory of one embodiment can include features of a synchronous flash device, as described in U.S. Patent Application No. 09/627,682 filed July 28, 2000, and incorporated herein by reference. The present decompression circuit increases efficiency while loading the volatile memory.

CONCLUSION

[0017] A processing system has been described that allows data downloads from a non-volatile memory to volatile memory. The non-volatile memory device includes a decompression engine to decompress the data prior to storing in the volatile memory. This built-in decompression circuit allows an increased amount of data to be stored in the flash. The compression operation is performed prior to initial storage in the flash memory.

[0018] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.